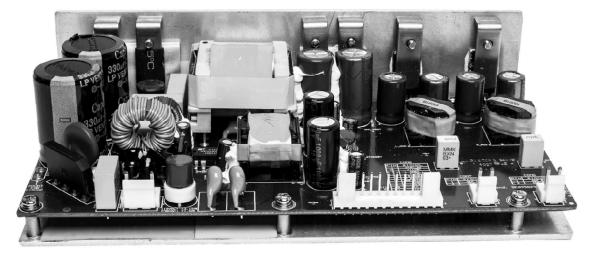


## PRODUCT DATA SHEET AUDIO LINE COMBINATION ALC0240-2300



# SCOPE

These technical specifications describes the functionalities and features of the Anaview Audio Line Combination ALC0240-2300, an integrated audio solution combining high-end amplifier and power supply technology, capable of delivering 2x120W FTC into 4 $\Omega$  @10%THD, 2x55W into 8 $\Omega$  @1%THD or 1x240W FTC into 8 $\Omega$  bridged. Instantaneous peak power 330W into 6 ohm bridged. Typical applications are audio receivers, powered speakers and residential audio system.

# Disclaimer

The data sheet contains specifications that may be subject to change without prior notice. Responsibility for verifying the performance, safety, reliability and compliance with legal standards of end products using this subassembly falls to the manufacturer of said end product.

ANAVIEW products are not authorized for use as critical components in life support devices or life support systems without the express written approval of the president of ETAL Group AB. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labelling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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# GENERAL

## **Environmental conditions**

Humidity	5 – 85% RH non condensing		
Operating Temperature Ambient	0°C to +55°C		
Storage Temperature	-40°C to +85°C		

## **Regulations and compliances**

	Emission	Designed to meet (*1) EN 55022 (2010) Class "B" FCC 15V Class "B" EN 61000-3-2 (2006) + A1 (2009) + A2 (2009) EN 61000-3-3 (2008) Tested at a level of 1/8 of the max output power.	
EMC	Immunity	IEC 61000-4-2 (2008) IEC 61000-4-3 (2006) + A1 (2007) + A2 (2010) IEC 61000-4-4 (2004) + A1 (2010) IEC 61000-4-5 (2005) IEC 61000-4-6 (2008) IEC 61000-4-8 (2009) IEC 61000-4-11 (2004)	
Safety	LVD	IEC 60065:2001 + A1:2005 + A2:2010 EN 60065:2002 + A1:2006 + A11:2008 + A2:2010 + A12:2011	
Power loss	EuP Energy Star	Designed to enable system compliance with: 2005/32/EC - 1275/2008: Standby/Off Mode Loss, Annex II Point Energy Star - Consumer Audio Products, Phase II	

(\*1) Additional filtering to MAINS INPUT is required to PASS Conducted Emission FCC 15V Class "B" and EN 55022 Class "B". See page 18.

#### Miscellaneous product specifications

Cooling	Convection cooling		
Mounting of the unit	See Figure 1 Board outline, dimensions (page 8).		
IEC Protection Class	Class II - Double insulation		
Efficiency	84% at 230Vac, 1KHz 2x50W into 8Ω		
Idle power consumption	9W typ. (10W max) at 230VAC		
Standby mode power consumption	<300mW when remote shut down by DISABLE input and no load. <500mW when supplying the 30mA on the +5V standby output		
Manufacturing according to workmanship standard	IPC-A-610, Revision D, February 2005		

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# **ELECTRICAL SPECIFICATIONS**

## Input specifications:

	Newsinglastic sectors 115 (220	N/A C		
Mains input voltage (*1)	Nominal rating: 115 / 230 Absolute min/max: 88-132 / 1	76-264 VAC		
Mains input freq	45-63 Hz			
Starting voltage 115V setting (*2)	<88VAC			
Starting voltage 230V setting (*2)	<196VAC			
Under voltage lockout level 115V setting (*2)	<78VAC			
Under voltage lockout level 230V setting (*2)	<156VAC			
DISABLE	Discrete input signal. Active high. Disable voltage: >3VDC (min) <15VDC (abs max) Max sourcing current needed : 200uA Inhibit disable : Leave pin unterminated or put to GND <3VDC (max)			
AMP_DISABLE	Discrete input signal. Active high. Disable voltage: >2.5VDC (min) <15VDC (abs max) Max sourcing current needed : 50uA Inhibit disable : Leave pin unterminated or put to GND <1.5VDC (max)			
IN_L+/_L-	0 - 1.39Vrms max (*3)Balanced audio input, left channel			
IN_R+/_R-	0 - 1.39Vrms max (*3)Balanced audio input, right channel			
Input impedance (*4)	Single ended input signal IN_L+ (CON2:10) Signal IN_L- (CON2:11) Ground Input impedance = 12k IN_R+ (CON2:12) Signal IN_R- (CON2:13) Ground Input impedance = 3k8 Input signal ground must also be connected to GND (CON2:8,9) to avoid large potential difference between ALC0240-2300 and source, since ALC0240-2300 is floating (not connected to protective earth).	Balanced input signal IN_L+ (CON2:10) Signal+ IN_L- (CON2:11) Signal- GND (CON2:8,9) Signal Ground Input impedance L+ = 12k Input impedance L- = 2k3 IN_R+ (CON2:12) Signal+ IN_R- (CON2:13) Signal- GND (CON2:8,9) Signal Ground Input impedance R+ = 2k3 Input impedance R- = 12k		

(\*1) (\*2) Mains AC input voltage range selectable with jumper.

- Measured without generating output power.
- At 230VAC mains input voltage. Maximum signal input voltage is given by output (\*3) power rating factor, as described in the Output Specifications.
- (\*4) Signal source output impedance must be symmetrical for IN+ and IN- on both channels or there will be a difference in gain between the channels and common mode rejection will be compromised. (see application notes for more information)

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## **Output** specifications:

Audio outputs (*1)(*2)	Max output voltage	Typ. cont. output power	Typ. output power FTC cond. (*3)	Max output power	Instantaneous peak output power	THD
	SE mode					
	0- 20Vrms	2x12.5W 4Ω	2x100W 4Ω 2x55W 8Ω	2x100W 4Ω 2x55W 8Ω	2x200W 4Ω 2x110W 8Ω	1%
OUT_L+/_L- OUT_R+/_R-	0- 22Vrms	2812.500 452	2x120W 4Ω 2x65W 8Ω	2x120W 4Ω 2x65W 8Ω	2x200W 4Ω 2x110W 8Ω	10%
	BTL mode					
	0- 28.3Vrms	22.5W 8Ω	200W 8Ω	200W 8Ω	270W 8Ω	1%
	0- 31Vrms	22.378 832	240W 8Ω	240W 8Ω	320W 8Ω	10%

Mains input voltage 115/230VAC. Output power of RMS load current. Due to the non-(\*1) regulated nature of the internal PSU, the output power depends on the mains input voltage. Hence the power rating follows the equation: % Power change = (% voltage change)<sup>2</sup>

(\*2) Both channels driven

(\*3) Test conditions: 1 hour pre heating with 1/8 of specified load and subsequently 5 min. with specified load at 120/230Vac, 1kHz input, T amb 25'C open and still air. Board mounted vertically.

	Nom.	. Voltage fluctuation		I Max	Voltage	
AUX outputs	voltage	Min (*1)	Max (*1)	cont. (*2)	ripple (*3)	Comments
AUX output supply voltage V1: (STBY_DC)	+5.0VDC			30mA	200mVp-p	(*4)
AUX output supply voltage V2: +11VDC	+11.0VDC	+10.5VDC	+13.0VDC	730mA	200mVp-p	
AUX output supply voltage V3: +5VDC	+5.0VDC	+4.75VDC	+5.35VDC	1450m A	200mVp-p	

(\*1) Max output on the +5VDC output occurs when it is loaded at min. and the +11VDC output is loaded at max. Vice versa for the +11VDC output.

(\*2) Peak loads up to 880mA is allowed for time frames less than 10sek. This is a thermal limitation which also restricts how frequent this load/time frame can occur.

- Measured with an oscilloscope probe which is soldered directly to the PCB. The oscilloscope (\*3) bandwidth shall be set to 20MHz.
- (\*4) The STBY\_DC output needs a minimum load of ~3mA at all times for unit to operate at all different load conditions and audio output power levels.

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## Maximum load for Energy Star compliance:

Compliance	Comment	STBY_DC	+11V	+5V	
Energy star	Maximum load to ensure <10W total idle consumption. Measured at 115/230VAC	30	170	340	mA

#### **Protections and functions:**

Mains input fuse	T1.6AE (time lag, enhanced BC) at	230 /AC (upper AC volt range)		
Mains input ruse	T3.15AL (time lag, low BC) at 115VAC (lower AC voltage range)			
Over voltage protection	Amplifier shut down during over voltage on output voltage rails. This can happen if the mains voltage exceeds the maximum rated level or during railpumping (due to DC on inputs or when generating subsonic frequencies). Immediately when the voltage has decreased the amplifier will start again. This protection mode will be heard as very short interrupts to the sound.			
Over current protection in amplifiers	<ul> <li>Treshold current : 9A (0.5Ω load, 1kHz burst). There are two modes of over current protection.</li> <li>1. Constant current mode. The output will behave as during voltage clipping i.e. the output voltage will be cut off on the top to maintain an allowed current.</li> <li>2. If the over current mode persists during a longer period (several periods of music) it is assumed that there is an error and the amplifier will shut down for a while and then restart.</li> </ul>			
Short circuit protection of	Over current limit	1630mA (*1)		
AUX output V2 +11VDC	Short circuit	Hick up mode		
Short circuit protection of	Over current limit	3000mA (*1)		
AUX output V3 +5.0VDC	Short circuit	Hick up mode		
Protection output status	Status output: CON2 Pin 6 "STATU Goes high during: 1. Over temperature shutdown 2. Over voltage shutdown	S"		
Remote shut down to standby mode	Shut down input: CON2 Pin 5 "DISABLE" Shut down by: Pull DISABLE input high (+3.5< <b>V</b> <+15VDC) Normal operation : Leave pin floating or put to GND (V<+1.5VDC) Startup time from release of DISABLE : 300ms			
Remote shut down of amplifier	Shut down input: CON2 Pin 7 "AMP_DISABLE" Shut down by: Pull DISABLE input high (+3.0 <v<+15 vdc)<br="">Normal operation : Leave pin floating or put to GND (V&lt;+1.0VDC) Startup time from release of AMP_DISABLE : 250ms</v<+15>			
Anti rail pumping	Startup time from release of AMP_DISABLE : 250ms Right audio input channel is internally inverted before amplification in order to consume power symmetrically from both power rails. This prevents rail pumping, since the bass of recordings is usually equally mixed into both channels. The output of the right channel is correspondingly internally inverted, such that this feature is transparent to the user. This is seen in fig. 2 When using one channel only it is still possible to generate full span			

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frequency that (DC being the	Hz into $4\Omega$ at nominal mains voltage. The lower is being generated the more the rails will be pumped extreme where even a few hundred millivolts can tage shutdown).
---------------------------------	---

(\*1) The +11VDC and +5VDC outputs are generated by a flyback converter which is current limited on the primary side. This means that the maximum output current on each output before drooping is the maximum output power (i.e. 15W) divided by the output voltage under test.

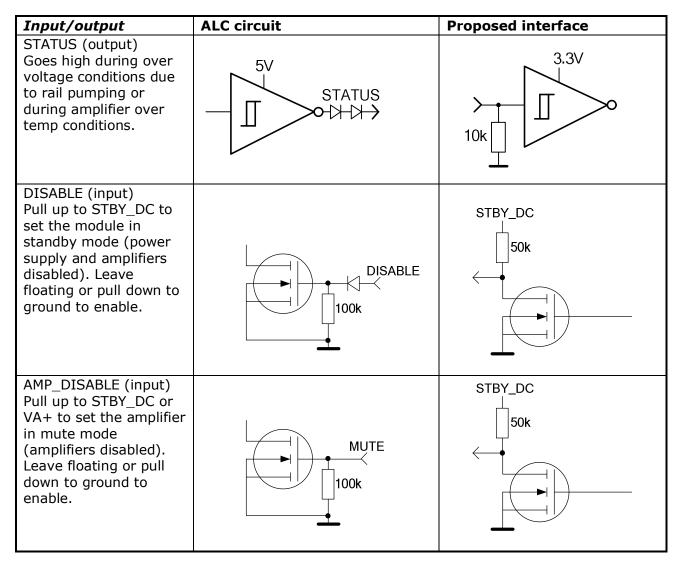
#### Audio specifications:

Offset voltage (open inputs)	5mV typ. (40mV max)
Switching frequency (idle)	430kHz typ. (410-450kHz min-max)
Switching residual	800mVpk
Recommended load	4Ω (SE mode) 8Ω (BTL mode)
Gain (f =1kHz)	24dB
Idle noise	30uV typ, 50uV max (A-weighted 20Hz < f < 20kHz)
Upper BW limit (-3dB)	60kHz
Lower BW limit (-3dB)	0Hz
Output impedance (100Hz)	3 mΩ
Residual noise vs freq	20Hz < f < 20KHz: -110dBV / 3uV (typ) Idle mode. See figure 3, page 9 - 90dBV / 32uV (max) -140dBV / 0.1uV TBD Amplifier shut down by AMP_DISABLE
Crosstalk vs freq	>=70dB, 20Hz to 20kHz. See figure 4 page 10
THD vs PWR	See figures 5-8 page 8 to 12
THD vs freq	See figure 9 page 12
Freq response	See figure 10 page 13

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## Proposed interfaces:



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# CONNECTIONS

Mains connector	CON1: 2 pin 0.312" (	7.92mm) locking header (JST B2P3-VH (LF) (SN))	
		nector : JST VHR-3N or similar	
	Pinning Pin1 : AC_N (Neutral) Pin2 : AC_L (Live)		
Signal connector	CON2:13pin 0.100" (	2.54mm) header (Molex 2227-2131)	
-	Suggested mating con	nector : Molex KK series 2695-13 or similar	
	Pinning:Description:Pin 1 : STBY_DCAUX output voltage V1 +5VDC (standby voltage)Pin 2 : +11VDCAUX output voltage V2 +11VDCPin 3 : GNDSecondary side ground.Pin 4 : +5VDCAUX output voltage V3 +5VDCPin 5 : DISABLEStandby input signal.Pin 6 : STATUSStatus output signal.Pin 7 : AMP_DISABLEAmplifier shutdown signalPin 8 : GNDSecondary side ground.Pin 9 : GNDSecondary side ground.Pin 10 : IN_L+Left audio channel positive inputPin 11 : IN_L-Left audio channel negative inputPin 12 : IN_R+Right audio channel negative inputPin 13 : IN_R-Right audio channel negative input		
Loudspeaker connectors	CON6 : 2pin 0.156" (3.96mm) header (JST B2P-VH (LF) (SN)) CON7 : 2pin 0.156" (3.96mm) header (JST B2P-VH (LF) (SN)) Suggested mating connector : JST VHR-2N or similar		
	<u>Pinning:</u> CON6 Pin1 : OUT_R+ Pin2 : OUT_R-	Description: Right audio channel positive output Right audio channel negative output	
	CON7 Pin1 : OUT_L+ Pin2 : OUT_L-	Left audio channel positive output Left audio channel negative output	

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## **MECHANICAL OUTLINE**

Size (l x w x h)	170x84.5x46mm, see <b>Figure 1</b> . Unit outline, dimensions below
Weight	420 gram
<b>IP figures, encapsulation</b> IP XY (X=Solids, Y=Liquids)	Open frame
Coloring, design and branding	ALC0240-2300

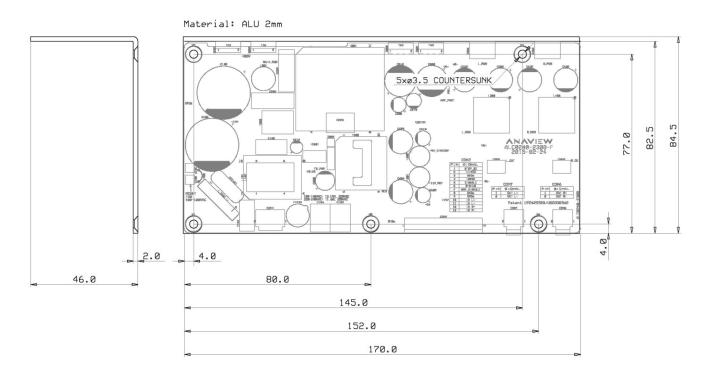
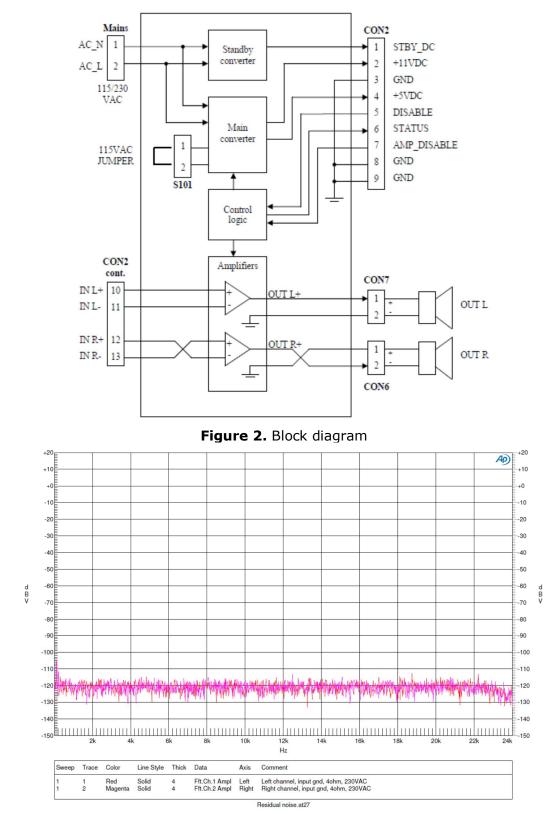


Figure 1. Unit outline, dimensions and mounting holes.

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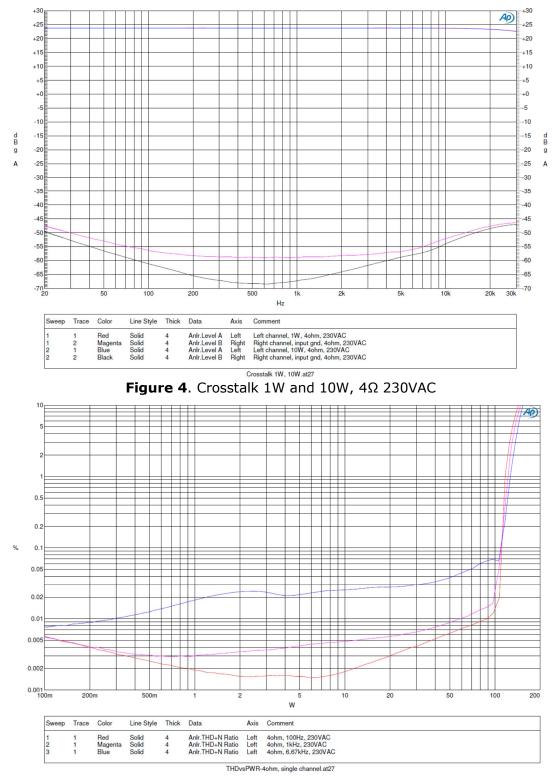


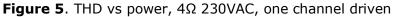




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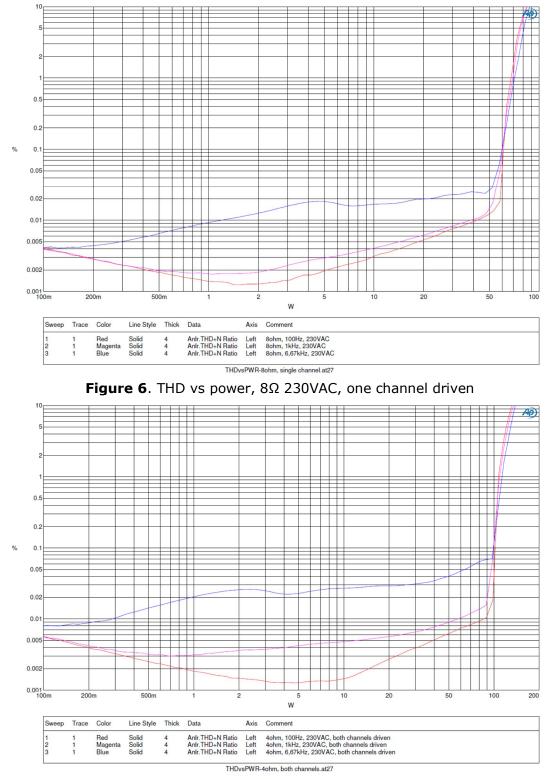


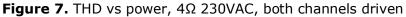




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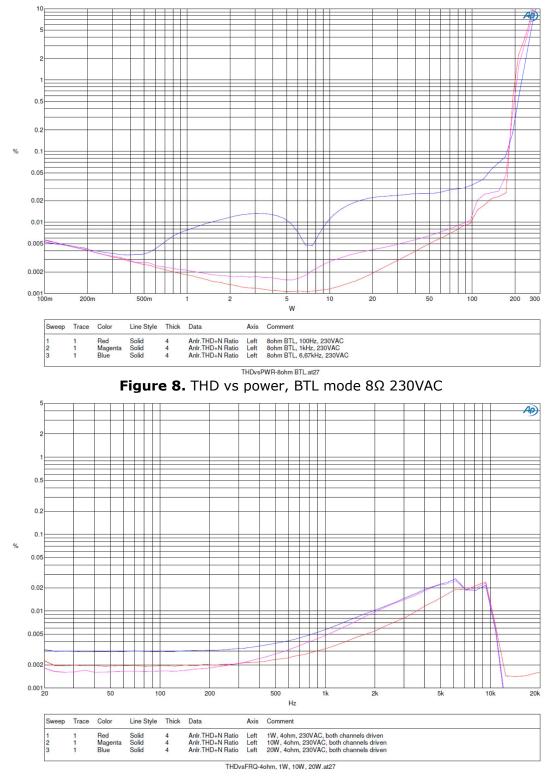


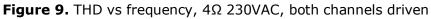




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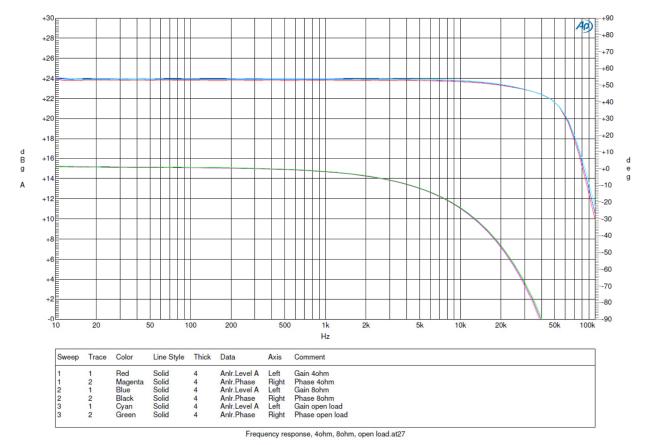


Figure 10. Frequency response, 230VAC, both channels driven.

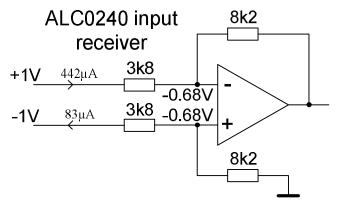
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## **APPLICATION NOTES**

#### **Optimizing input stage CMRR**

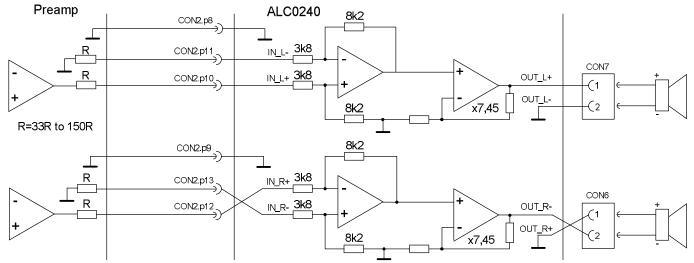
This is simplified drawing of the input of ALC0240. It is a typical circuit which is often used where the source impedance is well known and does not vary too much. Input currents are calculated when a balanced signal is applied. As can be seen the input impedance is not the same on both inputs and depending on which type of signal is applied (single ended or balanced) the input impedance changes.



This is however not a problem as long as a few precautions are made. Common mode rejection CMRR will be significantly improved by having the same source resistance on both the inputs.

#### Impedance balancing with single ended signal

Below is shown a setup with an impedance balanced single ended source. This requires a balanced cable.



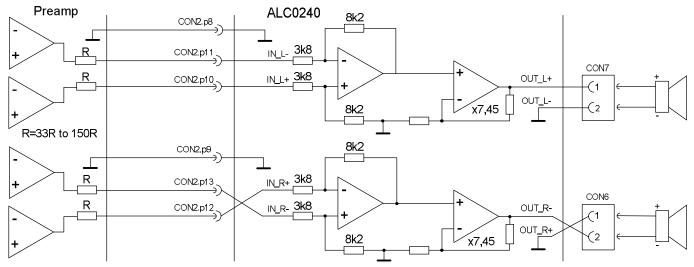
It is quite common to have a series resistance of 50ohm or more on the signal output so if the same resistance is placed in the opposite side of the signal of either sending or receiving side of the cable the CMRR rejection is intact.

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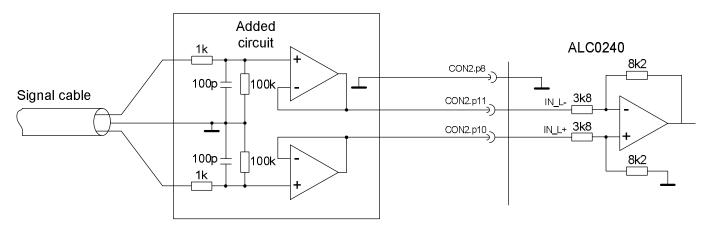


## Balanced input signal

If a balanced signal source is used the following setup applies.



If long cables are used the cable impedance itself can contribute in a non insignificant way to the series impedance and since that impedance is not very well defined (symmetrically) it can be an advantage to increase both the diff mode and common mode input impedance. In such a case an additional circuit as below can be added before the ALC module.

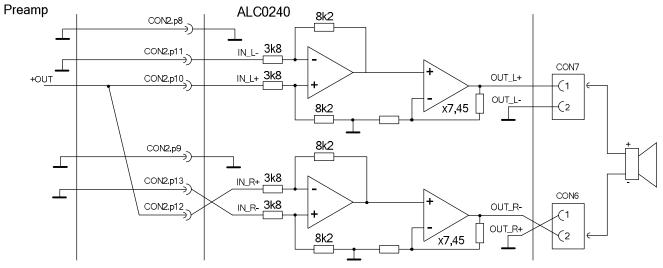


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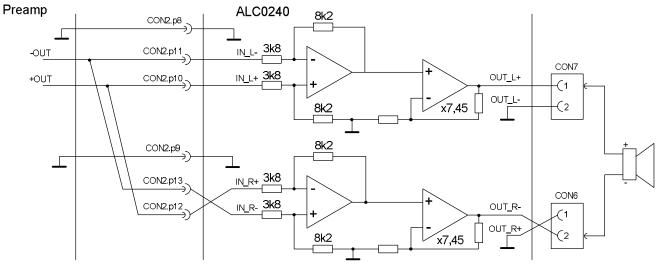


#### **BTL** setup

#### SE input signal



#### Balanced input signal



#### **IMPORTANT NOTE**

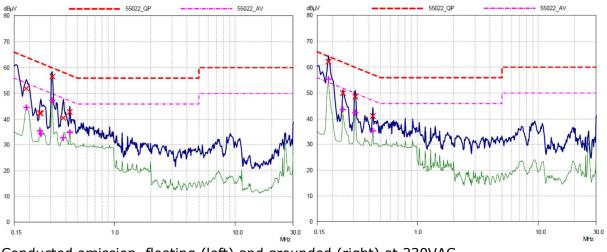
For proper function a  $\sim$ 5mA load must be applied to STBY\_DC, (con 2:pin 1). This is required since the flyback also powers the main power supply, and require a minimum load to the regulated outputs to deliver high enough voltage to the unregulated output on the primary side.

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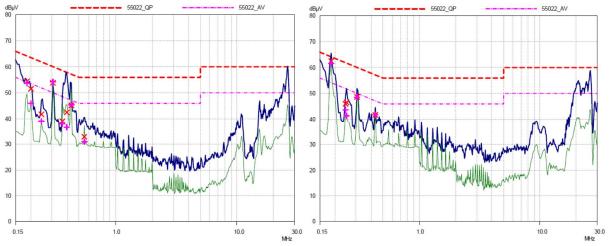


## **EMC MEASUREMENTS**

## **Conducted Emission**



Conducted emission, floating (left) and grounded (right) at 230VAC.



Conducted emission, floating (left) and grounded (right) at 115VAC. Disregard noise above 10MHz, generated by 115VAC-source.

ALC0240-2300 pass EN55022 Class "B" if left floating but fails if PE (Protective Earth) is connected, and fails FCC 15V Class "B" regardless of floating or PE connected. Additional Common Mode filtering is required to pass EN55022 Class "B" and FCC 15V Class "B" for all conditions, filtering required to pass depends on and shall be verified in end product.

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# **REVISION LOG**

Revision	Date	Item	Sign
A	2009-06-18	<ul> <li>Changed polarity of DISABLE input</li> <li>Added 230Vac input voltage to FTC test conditions</li> <li>Changed output voltage on AUX V2, max current on AUX V2-V3 and tolerance on AUX V3.</li> <li>Changed STATUS output voltage</li> <li>Increased gain and revised standby power consumption</li> <li>Added startup time from standby mode</li> <li>Revised idle noise and crosstalk</li> </ul>	KS
В	2010-01-25	<ul> <li>Updated description of DISABLE input</li> <li>Added mains input fusing data</li> <li>Updated board layout, fig. 1</li> <li>Added block diagram, fig 2</li> <li>Updated audio characteristics fig. 4-9, 11</li> </ul>	KS
С	2010-03-11	<ul> <li>Added input signal AMP_DISABLE to Input Spec and Protections and Functions.</li> <li>Updated note 3 in Output Spec</li> <li>Updated part no. for CON2 and suggested mating connector</li> <li>Updated CON2 pinout Added weight</li> <li>Updated residual noise spec and fig. 3</li> <li>Updated block diagram, fig. 2</li> </ul>	KS
D	2010-11-04	<ul> <li>Revised V2 and V3 output voltage spec, page 2</li> <li>Revised breaking capacity for the 1.6A fuse, page 2</li> <li>Decreased typ. switching freq to 430KHz</li> </ul>	KS
E	2011-03-01	<ul> <li>Revised performance graphs</li> </ul>	MC
F	2013-05-20	<ul> <li>Updated to Anaview standards. Start and stop voltage added in Electrical Specifications.</li> </ul>	MD/ PB
G	2013-05-22	<ul> <li>Updated Input Specifications.</li> <li>Revised contact information</li> </ul>	PB
Н	2014-04-03	<ul> <li>Added photo, disclaimer</li> <li>Updated input impedance info</li> <li>Added Energy Star compliance powers</li> <li>Updated thresholds in protections section</li> <li>Updated pictures in interface section</li> <li>Added application notes</li> </ul>	PB
I	2014-07-10	<ul> <li>Updated Regulations and compliances table</li> <li>Added EMC measurements and note about conducted emission and need for external filtering to pass EMC</li> </ul>	MC
J	2016-01-13	– Figure 1 updated	RK
к	2016-07-22	<ul> <li>Corrected pin references on page 3 for input signals</li> <li>Added note about minimum load on STBY_DC</li> </ul>	МС

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## **ANAVIEW CONTACT INFORMATION**

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